

# Inductance-Enhanced High-Impedance Surfaces for Broadband Simultaneous Switching Noise Mitigation in Power Planes

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**Abstract.** Full wave electromagnetic simulation is used to study the application of high-impedance surfaces (HIS) in simultaneous switching noise (SSN) mitigation in power planes. The impact of the geometry on the performance of power planes with simple and inductance-enhanced HIS is investigated. A lumped-element compact model form, applicable to both types of power planes is developed. Good agreement is obtained between the modeled and simulated S-parameters of the power planes from DC to 4 GHz.

## I. INTRODUCTION

Modern computer systems and microprocessors utilize multilayer printed circuit boards (PCB). Some of these layers are used for the signal, while others are used for power distribution. In many PCBs the power is distributed over several layers. The minimum requirement for the power distribution network, however, is to have at least two power planes as shown in Fig. 1, where one plane carries the supply voltage  $V_{DD}$  and the other plane is connected to the reference voltage  $V_{ref}$  or ground (Gnd). The two power planes extend over the entire width and length of the PCB and, therefore, constitute a parallel-plate waveguide. At different locations, integrated circuits (ICs) containing mostly active devices are connected between the two planes as illustrated by the active device on via B (Fig. 1). At some locations, the active devices are connected to the signal layers using through-vias as illustrated by via A. When the active device on via A for example switches a sudden change of current consumption occurs at that location. One or more modes of the parallel-plate waveguide will be excited, causing voltage waves to propagate from via A through the waveguide system. These voltage waves would then affect the  $V_{DD}$  on the board, which in turn can lead to the disturbance of the voltage of the active device connected to via A itself or to that of other active devices on the board. This problem becomes acute when several active devices have to switch simultaneously. In this case the problem of mitigating SSN in power planes is reduced to suppressing resonant modes of a parallel-plate waveguide with finite width.

Traditional ways of mitigating these parallel-plate resonant modes consist of using decoupling capacitors between the two metallic plates of the traditional power plane pair [1]-[3]. The decoupling capacitors are expected to short the radiated waves that propagate as surface current (at

the substrate-metal interface) at microwave frequencies. Previous research work, however, has shown that the lead inductance of the discrete capacitors strongly limits their noise mitigation capability [2], [3], [4]. An improved version of this technique consists of using embedded capacitance, which is obtained by reducing the spacing between the two planes. The embedded capacitance provides slightly better high-frequency performance because of the absence of lead inductance, but does not suppress the intrinsic modes of the parallel-plate waveguide.

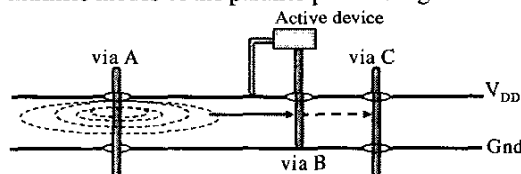


Fig. 1. Traditional power plane pair with connecting vias.

Most recently a new concept of mitigating SSN using a HIS [4] or an electromagnetic bandgap structure (EBG) [6] in place of the ground plane was proposed. This newly introduced concept offers an efficient blockage of the SSN all over the HIS or EBG structure and in all azimuthal directions, when the HIS is designed such that its forbidden bandgap contains the frequency range where the resonance of the simple power plane is dominant.

The purpose of this work is to investigate the qualitative relationships between the geometrical and electrical attributes of the novel power plane system. EM simulation capability is first established by achieving a good agreement with measured data in terms of S-parameters for a simple power plane. A number of simulations are then performed on power planes while varying the main physical (geometrical) parameters. A lumped-element compact model is then developed to enable the use of the proposed power plane in circuit simulators.

## II. VALIDATION OF THE EM SIMULATOR

Ansoft HFSS, an FEM based simulator, is used in this work. The validation of the simulator is established by comparing the simulated and measured S-parameters of a reference structure. Fig. 2 shows the S-parameter for a 10cm x 10cm power plane with and without decoupling capacitors (decaps) as described in [5] for noise mitigation. The total

height of the power plane is 1.54mm, and the dielectric constant is 4.4. The parasitic inductance and resistance of the decoupling capacitors are also taken into consideration. A very good agreement can be seen over the entire frequency range. As expected, the decoupling capacitors are only effective at low frequencies (<500MHz), where the impedance associated with the lead inductance of the discrete decoupling capacitors is negligible.

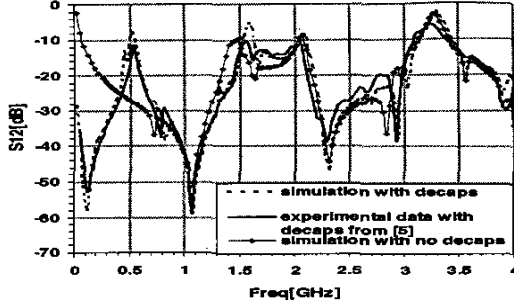


Fig. 2. Measured vs. simulated S-parameters of a power plane with and w/o decoupling capacitors.

### III. POWER PLANES USING HIS WITH STRAIGHT VIAS

#### A. Power plane geometry

The solid model of a typical power plane is shown in Fig. 3. It consists of a periodic high-impedance surface [7] that serves as ground plane and a solid metallic plate used as  $V_{DD}$  plane. The key geometrical parameters include the via to via distance or periodicity ( $a$ ) of the high-impedance surface, the via height ( $t$ ), the separation or gap ( $g$ ) between the patches, the patch width ( $w$ ) and the thickness ( $d$ ) of the dielectric material between the HIS and the top or  $V_{DD}$  plane. The width and length of the power plane, are fixed at 10cm x 10cm.

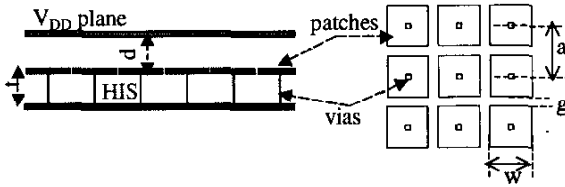


Fig. 3. Geometry of power plane with straight vias.

Once the simulation capability is established, physical parameters of interest are varied to find the optimized noise mitigation capability or to analyze the parameter sensitivity. To illustrate this, the geometrical parameters  $t$  and  $g$  are varied and the resultant changes of the S-parameters are evaluated. From the S-parameters, which in principle represent the frequency response of the power plane, the center frequency, the fractional bandwidth and the noise mitigation bandwidth, the maximum or minimum insertion loss in the stopband can be extracted.

#### A. Effect of Via height $t$

The first parameter to be studied is the via height. Fig. 4 shows the frequency response, when the via height is varied from 1.54mm to 4.62mm. All other geometrical parameters are fixed. In this case  $g=150\mu\text{m}$  and  $a=10\text{mm}$ . When  $t$  increases the center frequency as well as the corner frequencies of the stopband are shifted to lower frequencies. This decrease of the center frequency is associated with the increase in inductance, which is proportional to the via length. In fact the self-resonance frequency of the HIS is given as

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}, \quad (1)$$

where  $L$  and  $C$  represent the sheet inductance and sheet capacitance of the HIS respectively [7]. At the same time the fractional bandwidth (BW) does not decrease significantly. This is attributed to the fact that it is proportional to

$$BW \sim \sqrt{L/C}. \quad (2)$$

It is also important to notice that a significant increase of the via height is necessary to achieve noise mitigation in the hundreds MHz range.

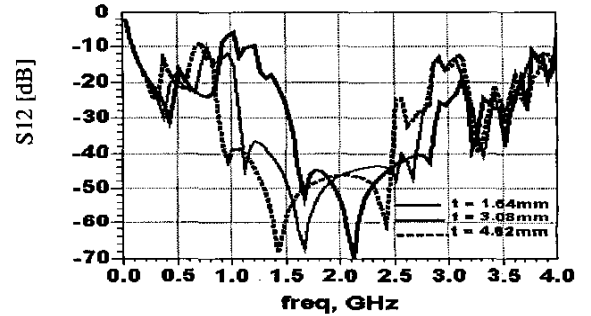


Fig. 4. Effect of via length on frequency response.

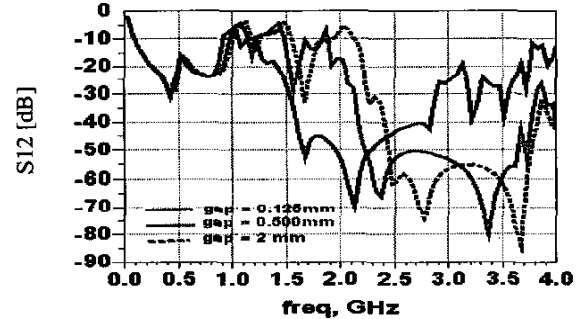


Fig. 5. Effect of patch separation on frequency response.

#### B. Effect of patch separation $g$

The patch separation  $g$  is varied from 2mm to 0.15mm with the via height fixed at 1.54mm. All other geometrical parameters are kept constant. The distance between the HIS

and the top plate is fixed at 1.54mm. A decrease  $\Delta g$  of the spacing corresponds to an increase  $\Delta w = \Delta g$  of the patch width. When the spacing  $g$  decreases, the fringing capacitance between adjacent patches increases, which in turn leads to an increase of the HIS sheet capacitance. This implies both a decrease of the center frequency and of the fractional bandwidth according to (1) and (2). Fig. 5 illustrates the impact of varying the spacing on the power plane performance.

#### IV. POWER PLANE USING INDUCTANCE-ENHANCED HIGH-IMPEDANCE SURFACE

##### A. Power plane with single-loop inductor in the HIS

As discussed in the previous paragraph, the use of a HIS with straight vias in power plane has two main limitations for low Gigahertz noise mitigation. First, large via lengths are required for lower frequencies, which would increase the thickness, weight and cost of the power planes. Second, the achievable fringing capacitance between the patches is limited by the technology. Capacitance-enhanced HIS were proposed in [7] and used in [6] for parallel-plate mode suppression in high-speed systems. This capacitance enhancement leads to a decrease of the fractional bandwidth. In [4], we proposed and used inductance-enhanced HIS for SSN mitigation in high-speed digital circuits. In that work, and as illustrated in Fig. 6, the single straight via of the HIS is replaced by a novel inductive element, which can be used to control the sheet inductance of the HIS.

With the total thickness of the power plane system (including the HIS) fixed at 1.54mm, the length of the single-loop inductor was varied from 5mm to 16mm. Fig. 7 shows the insertion loss for the two extreme cases. If we consider the -30dB bandwidth as the stopband of the powerplane, we notice that the fractional bandwidth increases with the loop length. At the same time there's a decrease in the bandwidth, suggesting that for any given structure the noise mitigation capability would also "saturate" as the inductance increases. More importantly resonance suppression is achieved down to 700MHz without any increase of the power plane thickness.

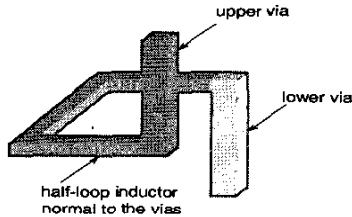


Fig. 6. Single-loop inductor for inductance enhancement.

##### B. Power plane with multi-turn inductor in the HIS

Instead of using a single loop inductor, a multi-turn inductor can be used to enhance the sheet inductance of the

HIS. By using a multi-turn or spiral inductor, the inductance per unit area is increased significantly. This is especially important if SSN mitigation below 1GHz is desired. Since the area required by the inductor is very small, unwanted coupling with adjacent cells is also minimized. The power plane frequency behavior is very similar to that of the power plane with single-loop inductor.

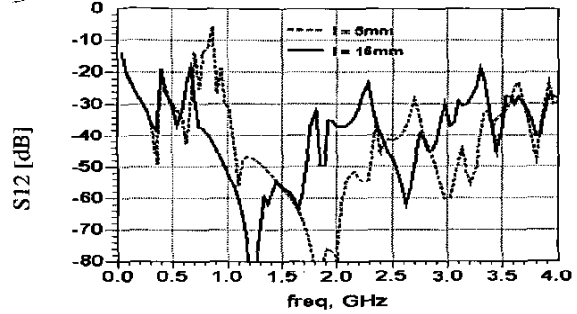


Fig. 7. Effect of inductor loop length on insertion loss.

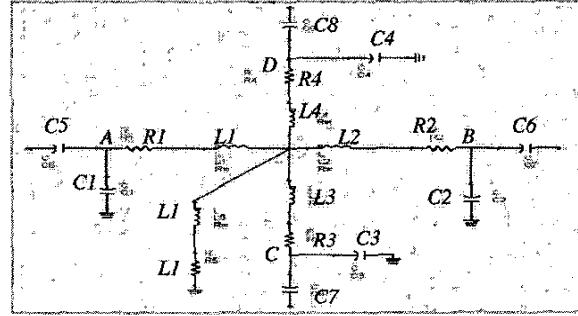


Fig. 8. Compact model the HIS unit cell

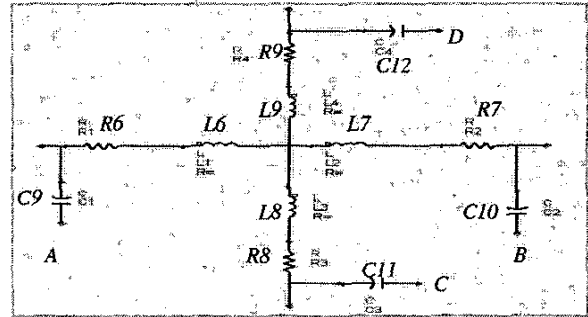


Fig. 9. Compact model of the top plate unit cell

#### V. COMPACT MODEL OF THE POWER PLANE

##### A. Model form definition

The compact model for the power plane is developed by first dividing it into unit cells. The compact model is then developed for the unit cell and several of them are cascaded into a 2-D array to build the model for the full power plane. For the planes presented in this work, the cell boundaries are

pre-defined by the periodicity of the HIS. Fig. 8 shows the proposed model form for the HIS unit cell. The RL-pairs R1L1 through R4L4, that each originate from the center of the patch, represent the impedance of the patch. The via is modeled by the RL-pair R5L5. The capacitors C1-C4 model the capacitive coupling between the patch and the bottom solid metallic plate. The capacitors C5-C8 model the capacitive coupling to the adjacent cell. The portion of the top plate directly above the HIS cell can be modeled with the compact model of Fig. 9. R6L6-R9L9 represent the impedance of the plate and C9-C12 represent the capacitance between the top plate and the HIS. The full model of the power plane unit cell is obtained by stacking the top plate and HIS models at nodes A-D. This compact model form can be used for power planes with simple HIS as well as for power planes with inductance- or capacitance-enhanced HIS. A rigorous derivation and the extension of this model form to other geometries is discussed in [8].

### B. Compact Model Validation

In order to validate the proposed model form for the power plane, a 10cm x 10cm power plane with the source at (5cm, 5cm) and the load at (5cm, 2cm) was simulated using HFSS. The compact model for the cascaded cells was then extracted using ADS. Fig. 10 shows the simulated vs. modeled S-parameters. A good agreement is obtained on the frequency range of interest.

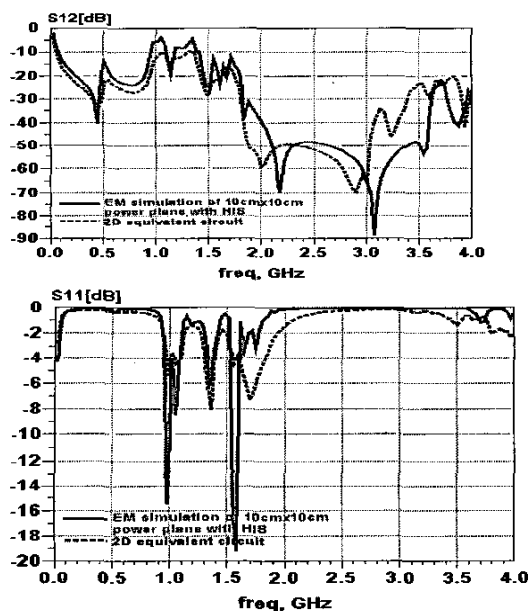


Fig. 10. Modeled vs. simulated S-parameters of a 10cmx10cm power plane.

## VI. CONCLUSION

The application of high-impedance electromagnetic surfaces in SSN mitigation has been investigated. While the via length may be a limiting factor for achieving low

frequency SSN mitigation with the conventional HIS, it was demonstrated that inductance-enhanced HIS can be designed for broadband mitigation of the SSN from the upper hundred MHz to the GHz frequencies. In addition a compact model form that enables the use and fast analysis of the power planes with HIS in circuit simulators was developed.

## ACKNOWLEDGEMENT

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